# Tutorial 02

Q1 Consider three diff erent processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

a.) Which processor has the highest performance expressed in instructions per second?

Performance of P1 (instructions/sec) = $3 * 10^9 / 1.5 = 2 * 10^9$
Performance of P2 (instructions/sec) = $2.5 * 10^9 / 1.0 = 2.5 * 10^9$
Performance of P3 (instructions/sec) = $4 * 10^9 / 2.2 = 1.8 * 10^9$

P2 has the highest performance

b.) If the processors each execute a program in 10 seconds, find the number of instructions.

Number of instructions (P1) = $10 * 2 * 10^9 = 2 * 10^{10}$
Number of instructions (P2) = $10 * 2.5 * 10^9 = 2.5 * 10^{10}$
Number of instructions (P3) = $10 * 1.8 * 10^9 = 1.8 * 10^{10}$

c.) We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

$CPI_{new} = CPI_{old} * 1.2$, then CPI (P1) = 1.8, CPI (P2) = 1.2, CPI (P3) = 2.64
Frequency (f) = No. instr. * CPI / time, then
P1: $f = 2 * 10^{10} * 1.8 / 7 = 5.14$ GHz
P2: $f = 2.5 * 10^{10} * 1.2 / 7 = 4.29$ GHz
P3: $f = 1.8 * 10^{10} * 2.64 / 7 = 6.79$ GHz

Q2 Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2. Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

a.) Which implementation is faster?

Class A: $10^5$ instr.
Class B: $2 * 10^5$ instr.
Class C: $5 * 10^5$ instr.
Class D: $2 * 10^5$ instr.
Time = No. instr. * CPI / clock rate

Total time P1 = $(10^5 + 2 * 10^5 * 2 + 5 * 10^5 * 3 + 2 * 10^5 * 3)/(2.5 * 10^9) = 10.4 * 10^{-4}$ s
Total time P2 = $(10^5 * 2 + 2 * 10^5 * 2 + 5 * 10^5 * 2 + 2 * 10^5 * 2)/(3.0 * 10^9) = 6.66 * 10^{-4}$ s

P2 is faster.

b.) What is the global CPI for each implementation?

CPI (P1) = $10.4 * 10^{-4} * 2.5 * 10^9 / 10^6 = 2.6$
CPI (P2) = $6.66 * 10^{-4} * 3.0 * 10^9 / 10^6 = 2.0$

Q3 The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power. The Core i5 Ivy Bridge, released in 2012, had a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that, on average, it consumed 30 W of static power and 40 W of dynamic power.

a.) For each processor find the average capacitive loads.

Capacitive load (C) = 2 * DP/($V^2$*F)
Pentium 4: C = 3.2E–8F
Core i5 Ivy Bridge: C = 2.9E–8F

b.) Find the percentage of the total dissipated power comprised by static power.

Pentium 4: 10/100 = 10%
Core i5 Ivy Bridge: 30/70 = 42.9%

Q4 Assume a program requires the execution of $50 \times 10^6$ FP instructions, $110 \times 10^6$ INT instructions, $80 \times 10^6$ L/S instructions, and $16 \times 10^6$ branch instructions. The CPI for each type of instruction is 1, 1, 4, and 2, respectively. Assume that the processor has a 2 GHz clock rate. By how much must we improve the CPI of FP instructions if we want the program to run two times faster (is it possible)?

Total execution time $= (50 \times 10^6 + 110 \times 10^6 + 4 \times 80 \times 10^6 + 2 \times 16 \times 10^6) / 2 \times 10^9$
$= 256 \times 10^{-3}$
New execution time $= 256 \times 10^{-3} / 2$
$= 128 \times 10^{-3}$
$CPI_{new} \times 50 \times 10^6 + 110 \times 10^6 + 4 \times 80 \times 10^6 + 2 \times 16 \times 10^6) / 2 \times 10^9 = 128 \times 10^{-3}$
$CPI_{new} \times 50 \times 10^6 = -206 \times 10^6$

It is not possible