

Design Automation on VLSI Systems

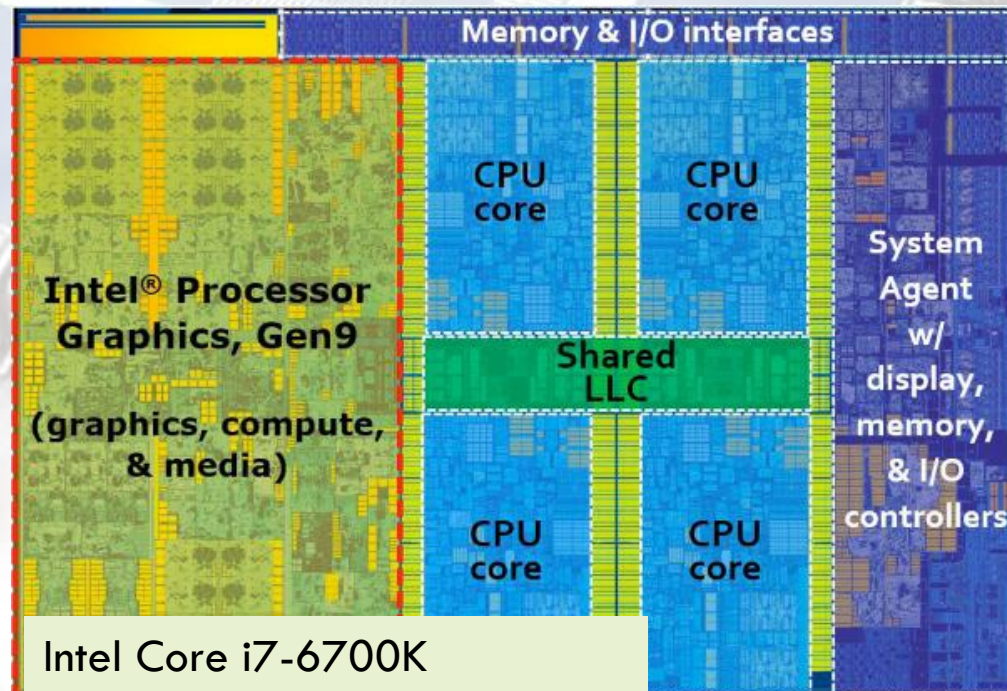
Dr. Bruce, Chiu-Wing Sham

Overview

- What is VLSI systems?
- What is design automation?

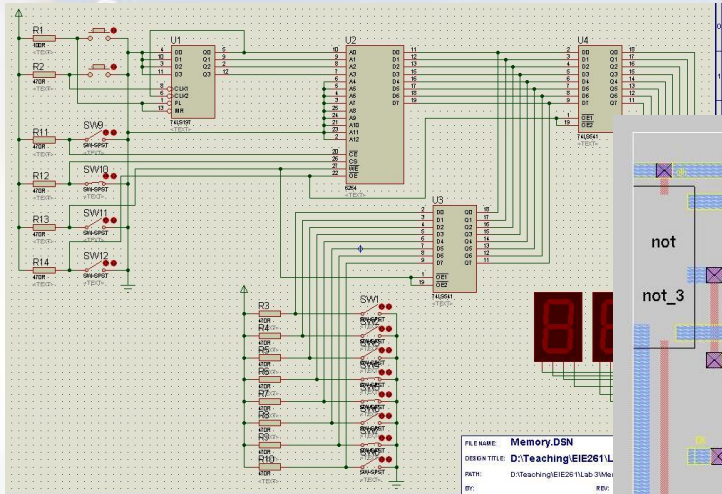
VLSI Systems

- Processors
- GPU
- Hardware Accelerators

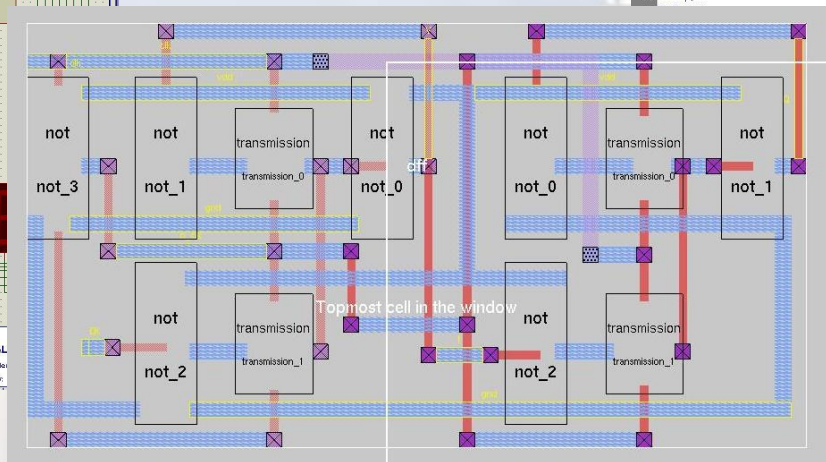


VLSI Systems

- Design procedure:
 - HDL (hardware descriptive language) design
 - Circuit diagram
 - Layout design

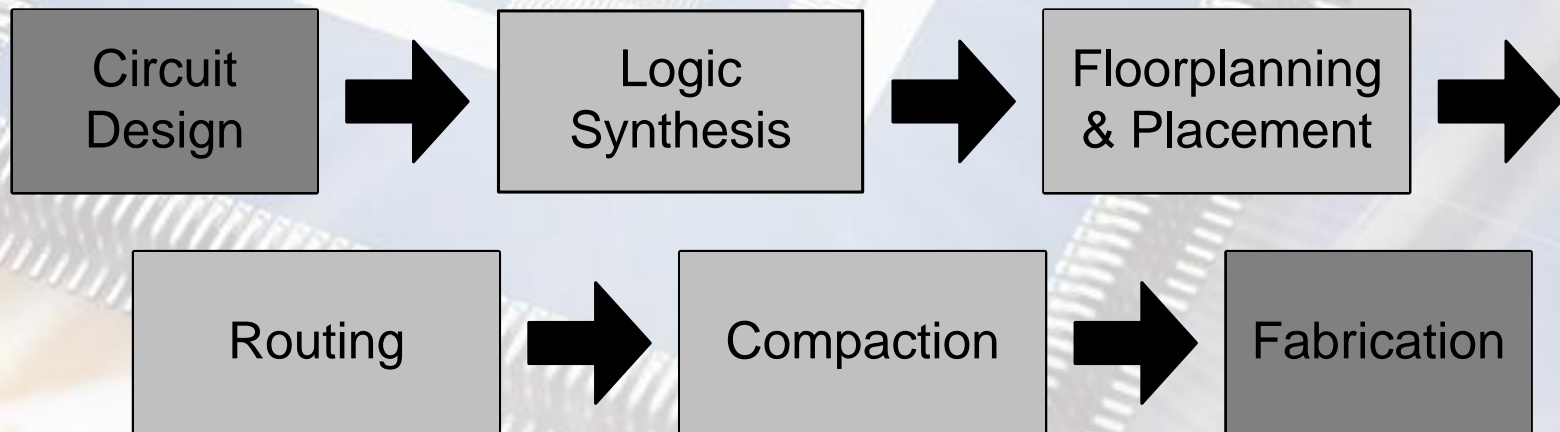


```
Test1 dff.vhd
7-- Module Name: addsub2 - Behavioral
8-- Project Name:
9-- Target Devices:
10-- Tool versions:
11-- Description:
12--
13-- Dependencies:
14--
15-- Revision:
16-- Revision 0.01 - File Created
17-- Additional Comments:
18--
19-----
20library IEEE;
21use IEEE.STD_LOGIC_1164.ALL;
22use IEEE.STD_LOGIC_ARITH.ALL;
23use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25Entity DFF is
26    port (
27        D: in std_logic;
28        S: in std_logic;
29        R: in std_logic;
30        C: in std_logic;
31        Q: out std_logic;
32        NQ: out std_logic
33    );
34end Entity;
```



Design Automation

- By using algorithms and heuristics, the layout can be automatically generated from the HDL



Design Automation

- Research Problems:
 - Logic Synthesis
 - Floorplanning and Placement
 - Routing

Logic Synthesis

- Goal:

- Create a logic gate network which performs a given set of functions

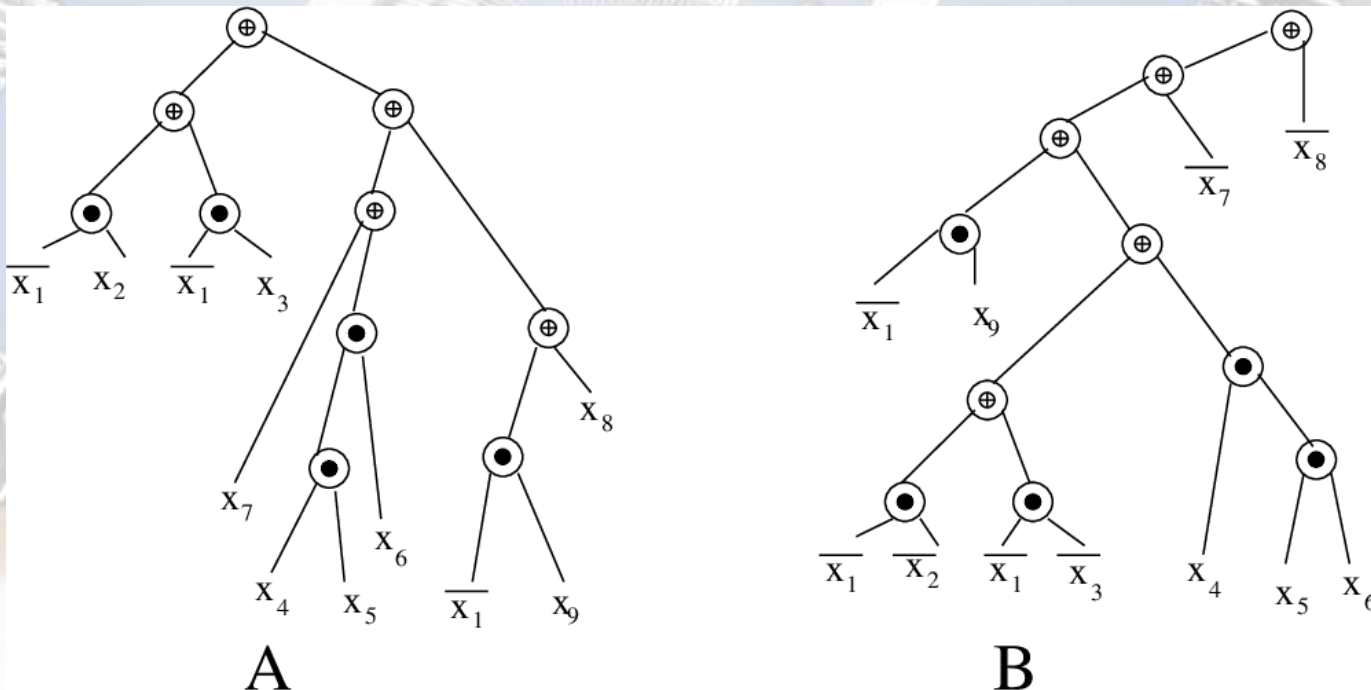
- Input are the Boolean formulas
- Outputs are the logic circuits

- Logic synthesis:

- Maps onto available gates or IP cores
- Restructures for the optimization of delay, area, testability, power, etc

Logic Synthesis

■ Example:

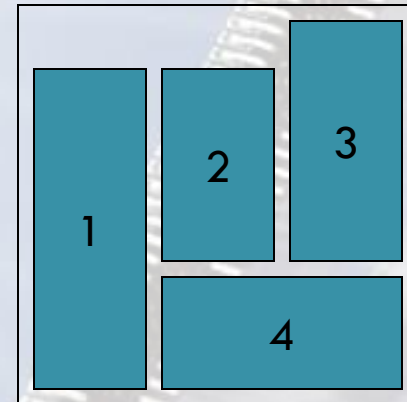
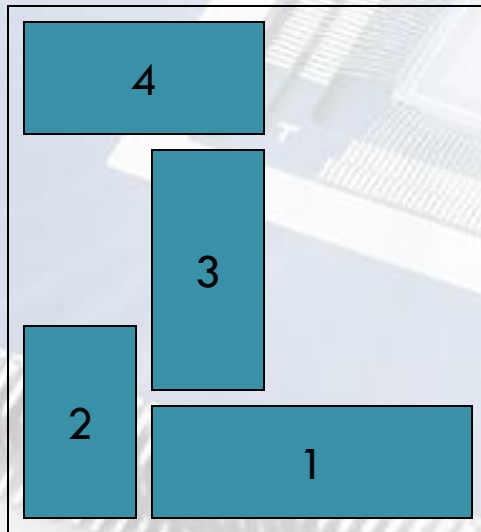


Floorplanning

- The floorplanning problem is to plan the positions and shapes of the blocks at the beginning of the design cycle to optimize circuit performance:
 - Chip area
 - Total wire length
 - Delay of critical path
 - Routability
 - Others, e.g., noise, heat dissipation, power consumption, etc

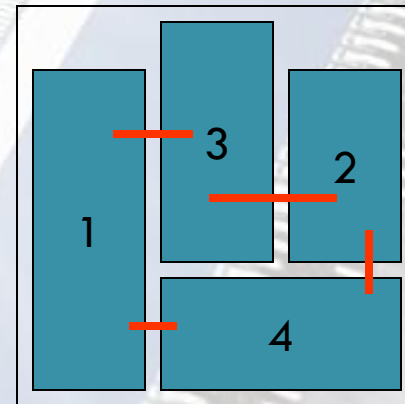
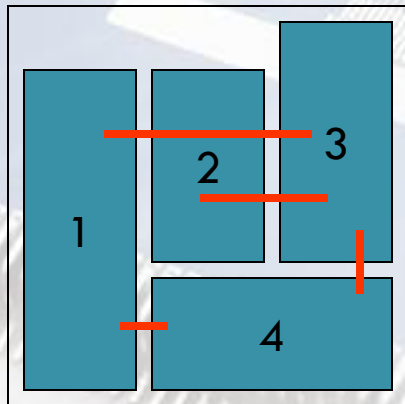
Floorplanning

- Example: (area)



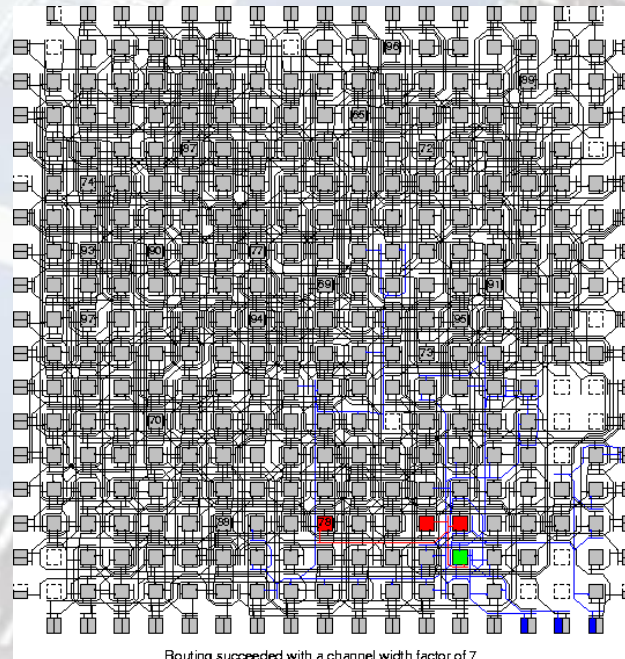
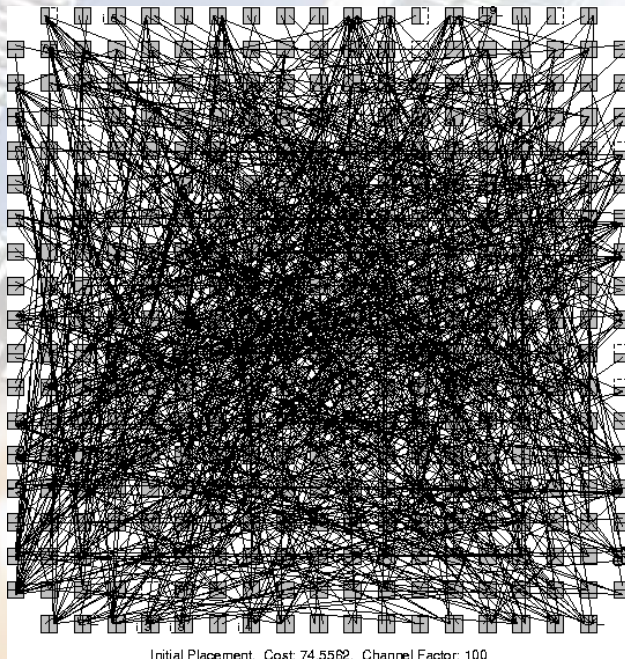
Floorplanning

- Example: (wire length)



Floorplanning

- Example: (routability)

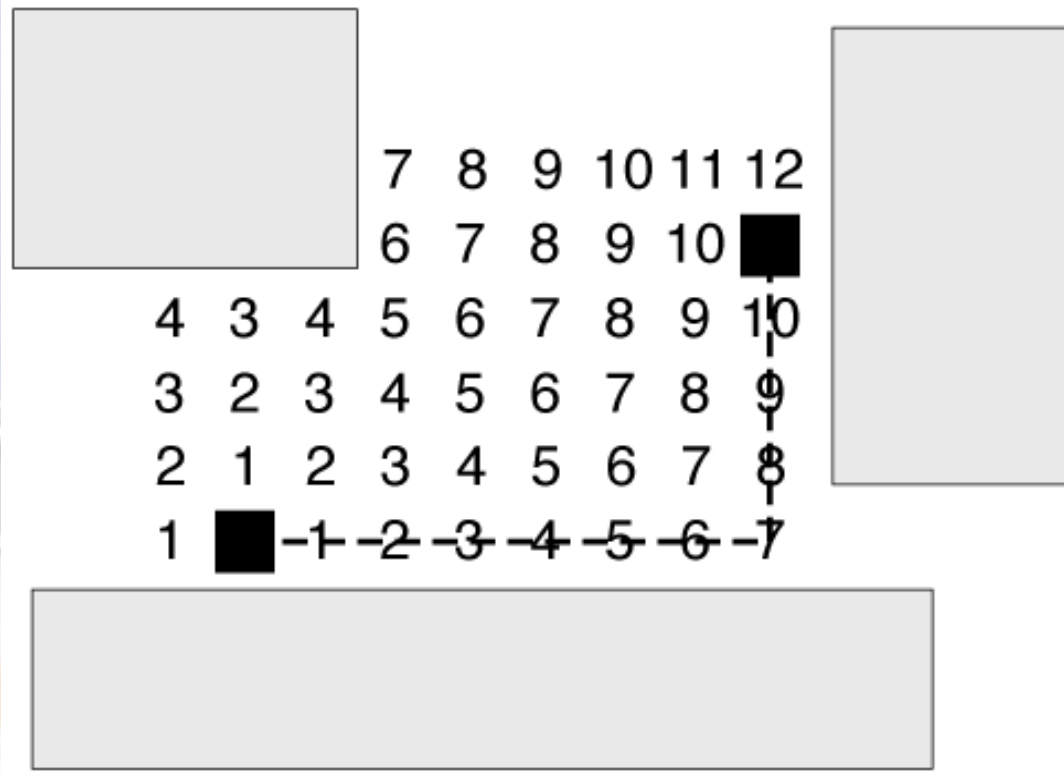


Routing

- Objective
 - 100% connectivity of a system
 - Minimize area
 - Minimize wirelength
- Constraints
 - Number of routing layers
 - Design rules
 - Timing (delay)
 - Crosstalk
 - Process variations

Routing

- Example: (maze routing)



Design Automation

- Industry Leaders in the world:
 - Cadence Design Systems
 - <http://www.cadence.com/>
 - Synopsys
 - <http://www.synopsys.com/>

Design Automation

- Research Progress:
 - ISPD contest
 - <http://ispd.cc/?page=contests>
 - ICCAD contest
 - <http://iccad-contest.org/2020/history.html>